# CD4093B Types

## CMOS Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

■ CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage $(V_P)$ and the negative voltage $(V_N)$ is defined as hysteresis voltage $(V_H)$ (see Fig. 2).

The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

■ Schmitt-trigger action on each input with no external components
■ Hysteresis voltage typically 0.9 V at $V_{DD}$ = 5 V and 2.3 V at $V_{DD}$ = 10 V
■ Noise immunity greater than 50%
■ No limit on input rise and fall times
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 $\mu$A at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

■ Wave and pulse shapers
■ High-noise-environment systems
■ Monostable multivibrators
■ Astable multivibrators
■ NAND logic



FUNCTIONAL DIAGRAM
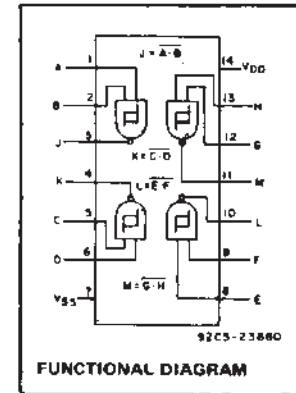
### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

| CHARACTERISTIC | MIN. | MAX. | UNITS |
|---|---|---|---|
| Supply Voltage Range (T$_A$ = Full Package Temp. Range) | 3 | 18 | V |

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, $(V_{DD})$
   Voltages referenced to V$_{SS}$ Terminal) .................................................. −0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ............................................... −0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT ....................................................... ±10mA
PACKAGE THERMAL IMPEDANCE, $\theta_{JA}$ (See Note 1):
   E package ............................................................................. 80°C/W
   M package ............................................................................. 86°C/W
   NS package ............................................................................ 76°C/W
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
   FOR T$_A$ = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ........................ 100mW
OPERATING-TEMPERATURE RANGE (T$_A$) ..................................................... −55°C to +125°C
STORAGE TEMPERATURE RANGE (T$_{stg}$) .................................................... −65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
   At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ...................... +265°C

NOTE 1:  Package thermal impedance is calculated in accordance with JESD 51-7.
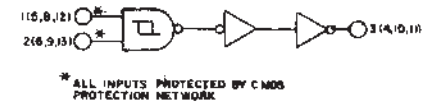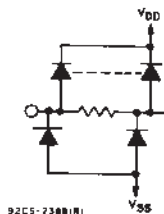


* ALL INPUTS PROTECTED BY CMOS PROTECTION NETWORK
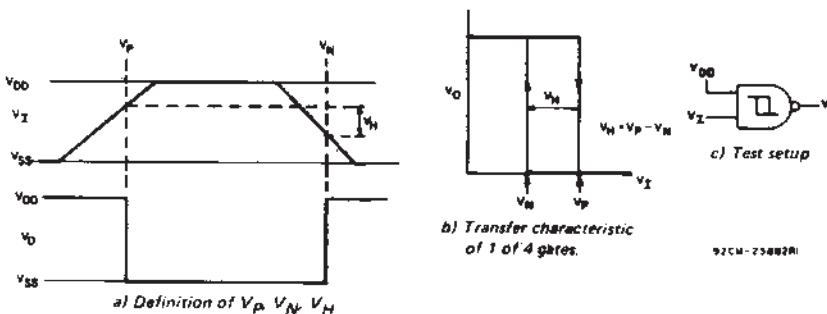
Fig. 1 – Logic diagram—1 of 4 Schmitt triggers.



a) Definition of $V_P$, $V_N$, $V_H$

b) Transfer characteristic of 1 of 4 gates.

c) Test setup

Fig. 2 – Hysteresis definition, characteristic, and test setup.
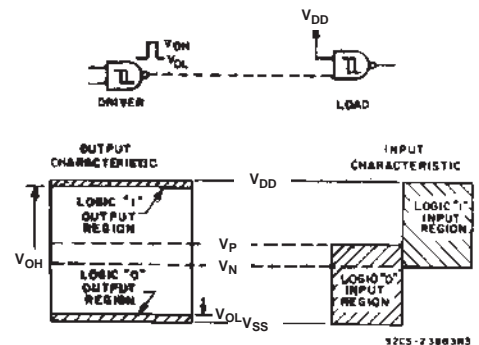


Fig. 3 – Input and output characteristics.

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**TEXAS INSTRUMENTS**

## CD4093B Types

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTER-ISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | +25 | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | MIN. | TYP. | MAX. | |
| Quiescent Device Current, $I_{DD}$ Max. | − | 0,5 | 5 | 1 | 1 | 30 | 30 | − | 0.02 | 1 | µA |
| | − | 0,10 | 10 | 2 | 2 | 60 | 60 | − | 0.02 | 2 | |
| | − | 0,15 | 16 | 4 | 4 | 120 | 120 | − | 0.02 | 4 | |
| | − | 0,20 | 20 | 20 | 20 | 600 | 600 | − | 0.04 | 20 | |
| Positive Trigger Threshold Voltage $V_P$ Min. | − | a | 5 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.9 | − | V |
| | − | a | 10 | 4.6 | 4.6 | 4.6 | 4.6 | 4.6 | 5.9 | − | |
| | − | a | 15 | 6.8 | 6.8 | 6.8 | 6.8 | 6.8 | 8.8 | − | |
| | − | b | 5 | 2.6 | 2.6 | 2.6 | 2.6 | 2.6 | 3.3 | − | |
| | − | b | 10 | 5.6 | 5.6 | 5.6 | 5.6 | 5.6 | 7 | | |
| | − | b | 15 | 6.3 | 6.3 | 6.3 | 6.3 | 6.3 | 9.4 | − | |
| $V_P$ Max. | − | a | 5 | 3.6 | 3.6 | 3.6 | 3.6 | − | 2.9 | 3.6 | V |
| | − | a | 10 | 7.1 | 7.1 | 7.1 | 7.1 | − | 5.9 | 7.1 | |
| | − | a | 15 | 10.8 | 10.8 | 10.8 | 10.8 | − | 8.8 | 10.8 | |
| | − | b | 5 | 4 | 4 | 4 | 4 | − | 3.3 | 4 | |
| | − | b | 10 | 8.2 | 8.2 | 8.2 | 8.2 | − | 7 | 8.2 | |
| | − | b | 15 | 12.7 | 12.7 | 12.7 | 12.7 | − | 9.4 | 12.7 | |
| Negative Trigger Threshold Voltage $V_N$ Min. | − | a | 5 | 0.9 | 0.9 | 0.9 | 0.9 | 0.9 | 1.9 | | V |
| | − | a | 10 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 3.9 | − | |
| | − | a | 15 | 4 | 4 | 4 | 4 | 4 | 5.8 | − | |
| | − | b | 5 | 1.4 | 1.4 | 1.4 | 1.4 | 1.4 | 2.3 | − | |
| | − | b | 10 | 3.4 | 3.4 | 3.4 | 3.4 | 3.4 | 5.1 | − | |
| | − | b | 15 | 4.8 | 4.8 | 4.8 | 4.8 | 4.8 | 7.3 | − | |
| $V_N$ Max. | − | a | 5 | 2.8 | 2.8 | 2.8 | 2.8 | − | 1.9 | 2.8 | V |
| | − | a | 10 | 5.2 | 5.2 | 5.2 | 5.2 | − | 3.9 | 5.2 | |
| | − | a | 15 | 7.4 | 7.4 | 7.4 | 7.4 | − | 5.8 | 7.4 | |
| | − | b | 5 | 3.2 | 3.2 | 3.2 | 3.2 | − | 2.3 | 3.2 | |
| | − | b | 10 | 6.6 | 6.6 | 6.6 | 6.6 | − | 5.1 | 6.6 | |
| | − | b | 15 | 9.6 | 9.6 | 9.6 | 9.6 | − | 7.3 | 9.6 | |
| Hysteresis Voltage $V_H$ Min. | − | a | 5 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.9 | − | V |
| | − | a | 10 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 2.3 | − | |
| | − | a | 15 | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 | 3.5 | − | |
| | − | b | 5 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.9 | − | |
| | − | b | 10 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 2.3 | − | |
| | − | b | 15 | 1.6 | 1.6 | 1.6 | 1.6 | 1.6 | 3.5 | − | |
| $V_H$ Max. | − | a | 5 | 1.6 | 1.6 | 1.6 | 1.6 | − | 0.9 | 1.6 | V |
| | − | a | 10 | 3.4 | 3.4 | 3.4 | 3.4 | − | 2.3 | 3.4 | |
| | − | a | 15 | 5 | 5 | 5 | 5 | − | 3.5 | 5 | |
| | − | b | 5 | 1.6 | 1.6 | 1.6 | 1.6 | − | 0.9 | 1.6 | |
| | − | b | 10 | 3.4 | 3.4 | 3.4 | 3.4 | − | 2.3 | 3.4 | |
| | − | b | 15 | 5 | 5 | 5 | 5 | − | 3.5 | 5 | |

a Input on terminals 1,5,8,12 or 2,6,9,13; other inputs to $V_{DD}$.

b Input on terminals 1 and 2, 5 and 6, 8 and 9, or 12 and 13; other inputs to $V_{DD}$.
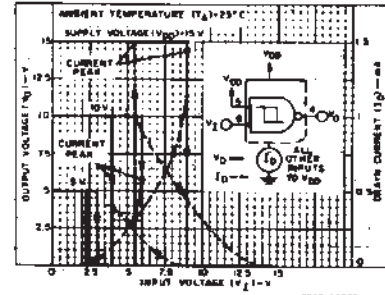


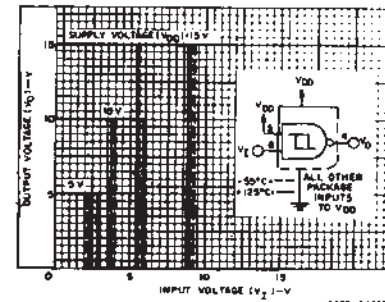Fig. 4 — Typical current and voltage transfer characteristics.



Fig. 5 — Typical voltage transfer characteristics as a function of temperature.
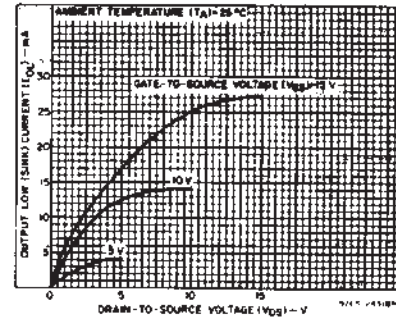


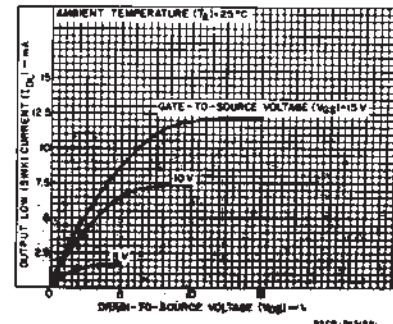Fig. 6 — Typical output low (sink) current characteristics.



Fig. 7 — Minimum output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS (CONT'D)

| CHARACTER-ISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $V_O$ (V) | $V_{IN}$ (V) | $V_{DD}$ (V) | −55 | −40 | +85 | +125 | +25 | | | |
| | | | | | | | | MIN. | TYP. | MAX. | |
| Output Low (Sink) Current, $I_{OL}$ Min. | 0.4 | 0.5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | − | mA |
| | 0.5 | 0,10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | − | |
| | 1.5 | 0,15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | − | |
| Output High (Source) Current, $I_{OH}$ Min. | 4.6 | 0.5 | 5 | −0.64 | −0.61 | −0.42 | −0.36 | −0.51 | −1 | − | |
| | 2.5 | 0.5 | 5 | −2 | −1.8 | −1.3 | −1.15 | −1.6 | −3.2 | − | |
| | 9.5 | 0.10 | 10 | −1.6 | −1.5 | 1.1 | −0.9 | −1.3 | −2.6 | − | |
| | 13.5 | 0,15 | 15 | −4.2 | −4 | −2.8 | −2.4 | −3.4 | −6.8 | − | |
| Output Voltage Low-Level, $V_{OL}$ Max. | − | 0.5 | 5 | 0.05 | | | | − | 0 | 0.05 | V |
| | − | 0,10 | 10 | 0.05 | | | | − | 0 | 0.05 | |
| | − | 0,15 | 15 | 0.05 | | | | − | 0 | 0.05 | |
| Output Voltage High-Level, $V_{OH}$ Min. | − | 0,5 | 5 | 4.95 | | | | 4.95 | 5 | − | |
| | − | 0,10 | 10 | 9.95 | | | | 9.95 | 10 | − | |
| | − | 0,15 | 15 | 14.95 | | | | 14.95 | | − | |
| Input Current, $I_{IN}$ Max. | − | 0,18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | − | ±$10^{-5}$ | ±0.1 | μA |

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$; Input $t_r$, $t_f$ = 20 ns, $C_L$ = 50 pF, $R_L$ = 200kΩ

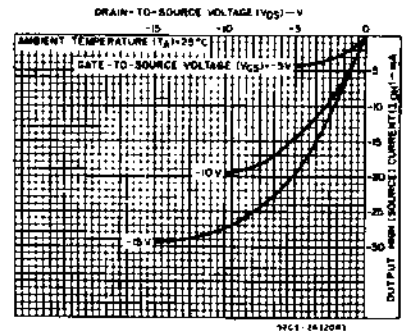| CHARACTERISTIC | TEST CONDITIONS | | LIMITS | | UNITS |
|---|---|---|---|---|---|
| | | $V_{DD}$ VOLTS | TYP. | MAX. | |
| Propagation Delay Time: $t_{PHL}$, $t_{PLH}$ | | 5 | 190 | 380 | ns |
| | | 10 | 90 | 180 | |
| | | 15 | 65 | 130 | |
| Transition Time, $t_{THL}$, $t_{TLH}$ | | 5 | 100 | 200 | ns |
| | | 10 | 50 | 100 | |
| | | 15 | 40 | 80 | |
| Input Capacitance, $C_{IN}$ | Any Input | | 5 | 7.5 | pF |



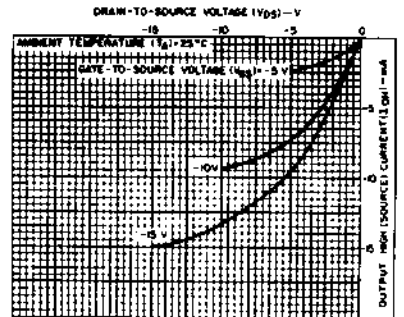Fig. 8 – Typical output high (source) current characteristics.



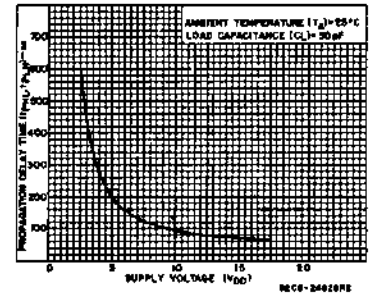Fig. 9 – Minimum output high (source) current characteristics.



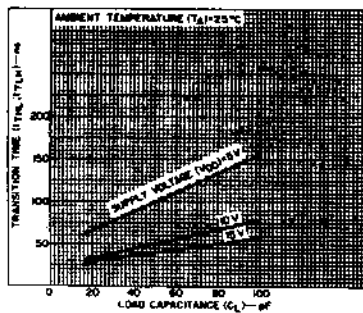Fig. 10 – Typical propagation delay time vs. supply voltage.



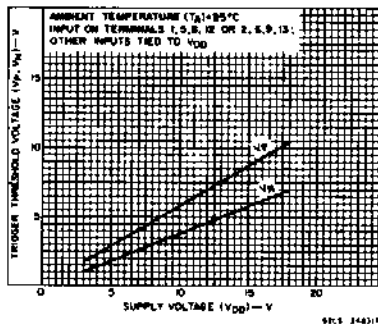Fig. 11 – Typical transition time vs. load capacitance.
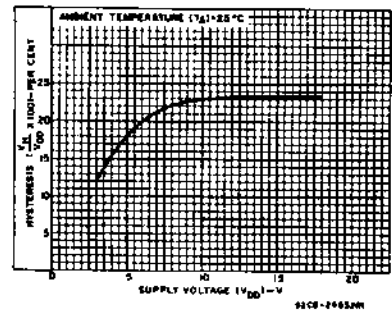


Fig. 12 – Typical trigger threshold voltage vs. $V_{DD}$.



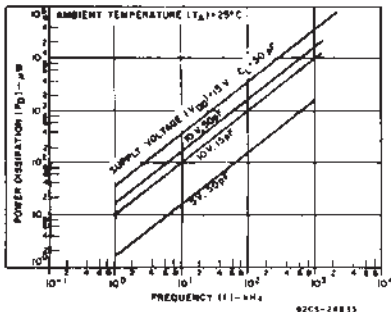Fig. 13 – Typical per cent hysteresis vs. supply voltage.

3

Fig. 14 — Typical power dissipation vs. frequency characteristics.



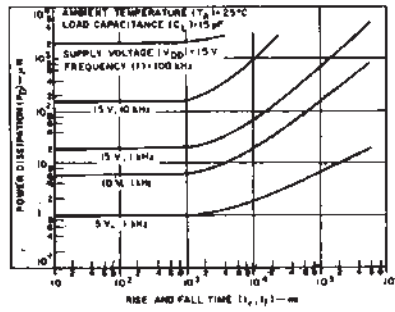Fig. 15 — Typical power dissipation vs. rise and fall times.

APPLICATIONS

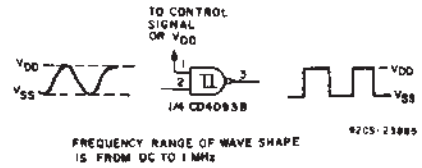

FREQUENCY RANGE OF WAVE SHAPE IS FROM DC TO 1 MHz

Fig. 16 — Wave shaper.



$$t_M = RC \ln\left(\frac{V_{DD}}{V_{DD}-V_P}\right)$$

$$50\,k\Omega \leq R \leq 1\,M\Omega$$
$$100\,pF \leq C \leq 1\,\mu F$$

FOR THE RANGE OF R AND C GIVEN $5\,\mu s < t_M < 1s$

Fig. 17 — Monostable multivibrator.



$$t_A = RC \ln\left(\frac{V_P}{V_N}\right)\left(\frac{V_{DD}-V_N}{V_{DD}-V_P}\right)$$

$$50\,k\Omega \leq R \leq 1\,M\Omega$$
$$100\,pF \leq C \leq 1\,\mu F$$

FOR THE RANGE OF R AND C GIVEN $2\,\mu s < t_A < 0.4s$
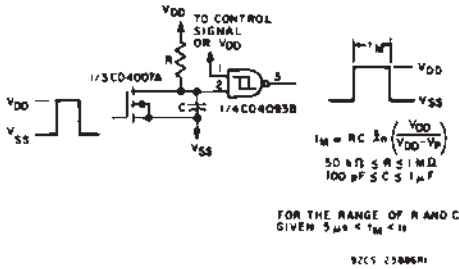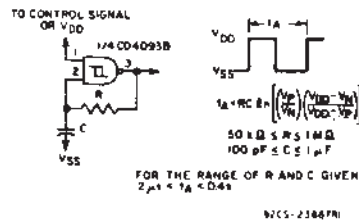
Fig. 18 — Astable multivibrator.
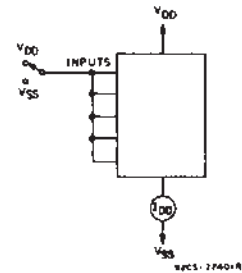


Fig. 19 — Quiescent device current test circuit.



NOTE
MEASURE INPUTS SEQUENTIALLY, TO BOTH $V_{DD}$ AND $V_{SS}$ CONNECT ALL UNUSED INPUTS TO EITHER $V_{DD}$ OR $V_{SS}$
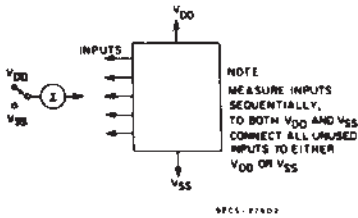
Fig. 20 — Input current test circuit.



(TOP VIEW)

TERMINAL ASSIGNMENT
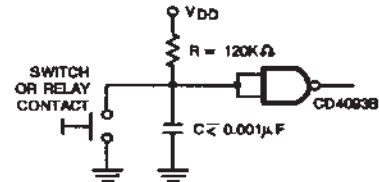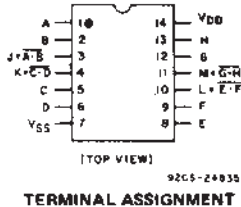


Fig. 21 — Contact Debouncer

4

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 7704602CA | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7704602CA CD4093BF3A | Samples |
| CD4093BE | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4093BE | Samples |
| CD4093BEE4 | ACTIVE | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4093BE | Samples |
| CD4093BF | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD4093BF | Samples |
| CD4093BF3A | ACTIVE | CDIP | J | 14 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 7704602CA CD4093BF3A | Samples |
| CD4093BM | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093BM | Samples |
| CD4093BM96 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093BM | Samples |
| CD4093BM96E4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093BM | Samples |
| CD4093BM96G4 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093BM | Samples |
| CD4093BMG4 | ACTIVE | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093BM | Samples |
| CD4093BMT | ACTIVE | SOIC | D | 14 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093BM | Samples |
| CD4093BNSR | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093B | Samples |
| CD4093BNSRG4 | ACTIVE | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4093B | Samples |
| CD4093BPW | ACTIVE | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM093B | Samples |
| CD4093BPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM093B | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

[2] **RoHS:**  TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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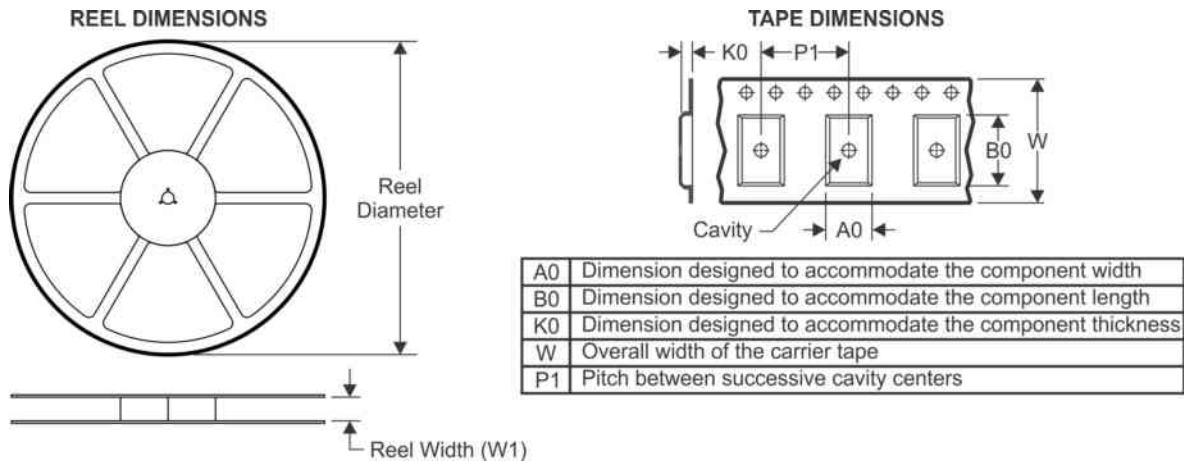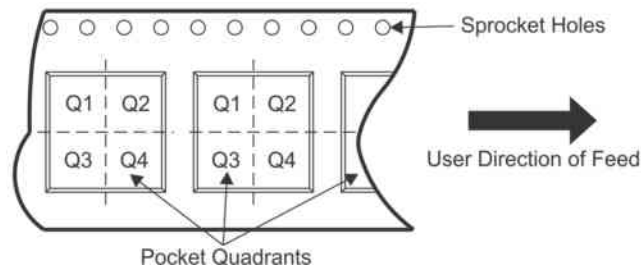**OTHER QUALIFIED VERSIONS OF CD4093B, CD4093B-MIL :**

● Catalog : CD4093B

● Automotive : CD4093B-Q1, CD4093B-Q1

● Military : CD4093B-MIL

NOTE: Qualified Version Definitions:

　　● Catalog - TI's standard catalog product

　　● Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



**REEL DIMENSIONS**

Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**

| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4093BM96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4093BMT | SOIC | D | 14 | 250 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CD4093BNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4093BPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**
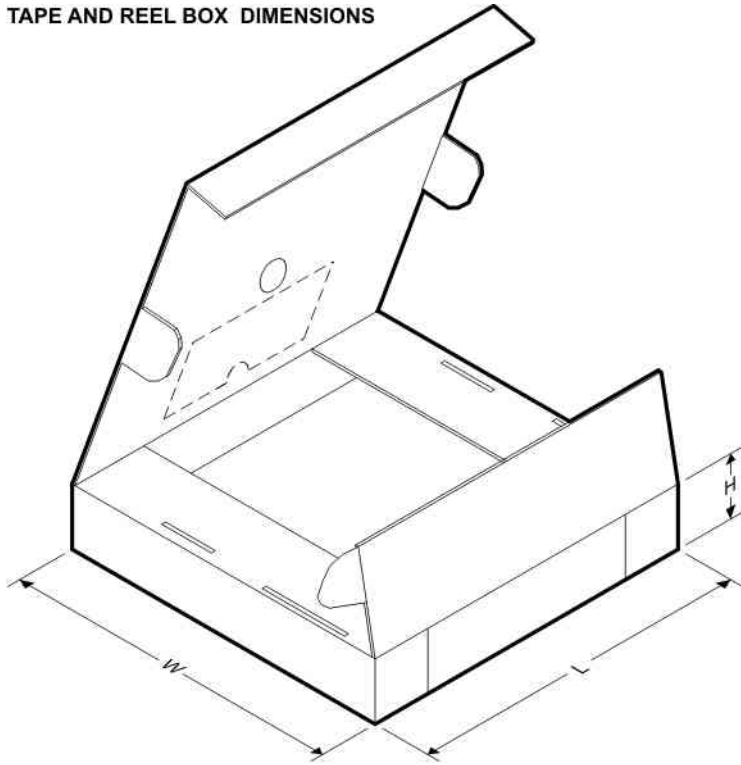
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| CD4093BM96 | SOIC | D | 14 | 2500 | 853.0 | 449.0 | 35.0 |
| CD4093BMT | SOIC | D | 14 | 250 | 210.0 | 185.0 | 35.0 |
| CD4093BNSR | SO | NS | 14 | 2000 | 853.0 | 449.0 | 35.0 |
| CD4093BPWR | TSSOP | PW | 14 | 2000 | 853.0 | 449.0 | 35.0 |

**NS (R-PDSO-G**)**                           **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

| PINS ** DIM | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A  MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A  MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03
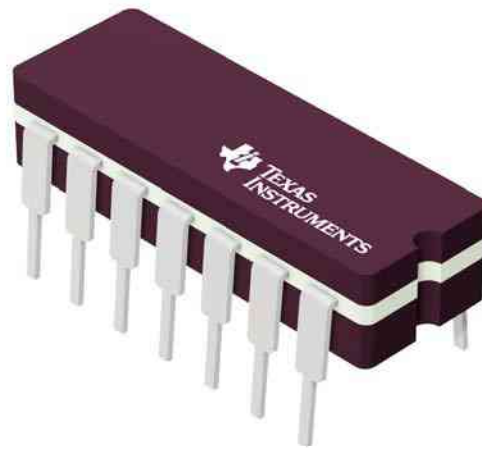
NOTES:   A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

PIN 1 ID
(OPTIONAL)

A

4X .005 MIN
[0.13]

.015-.060  TYP
[0.38-1.52]

1

14

12X  .100
[2.54]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕  .010 [0.25] C A B

.754-.785
[19.15-19.94]

7

8

B

.245-.283
[6.22-7.19]

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015   GAGE PLANE
[0.38]

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for
   reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

(.300 ) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

1

14

12X (.100 )
[2.54]

SYMM
¢

14X (Ø .039)
[1]

7

8

SYMM
¢

## LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002 ) TYP
[0.05]

## DETAIL A
SCALE: 15X

METAL

(Ø .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

## DETAIL B
13X, SCALE: 15X

4214771/A   05/2017

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D (R−PDSO−G14)  PLASTIC SMALL OUTLINE



0.344 (8,75)
0.337 (8,55)
△C

14        8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) △D

1        7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)    0°–8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M  06/11

NOTES:  A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
△D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS−012 variation AB.

D (R−PDSO−G14)                                    PLASTIC  SMALL  OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E  08/12

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G14)                              PLASTIC SMALL OUTLINE



4040064−3/G  02/11
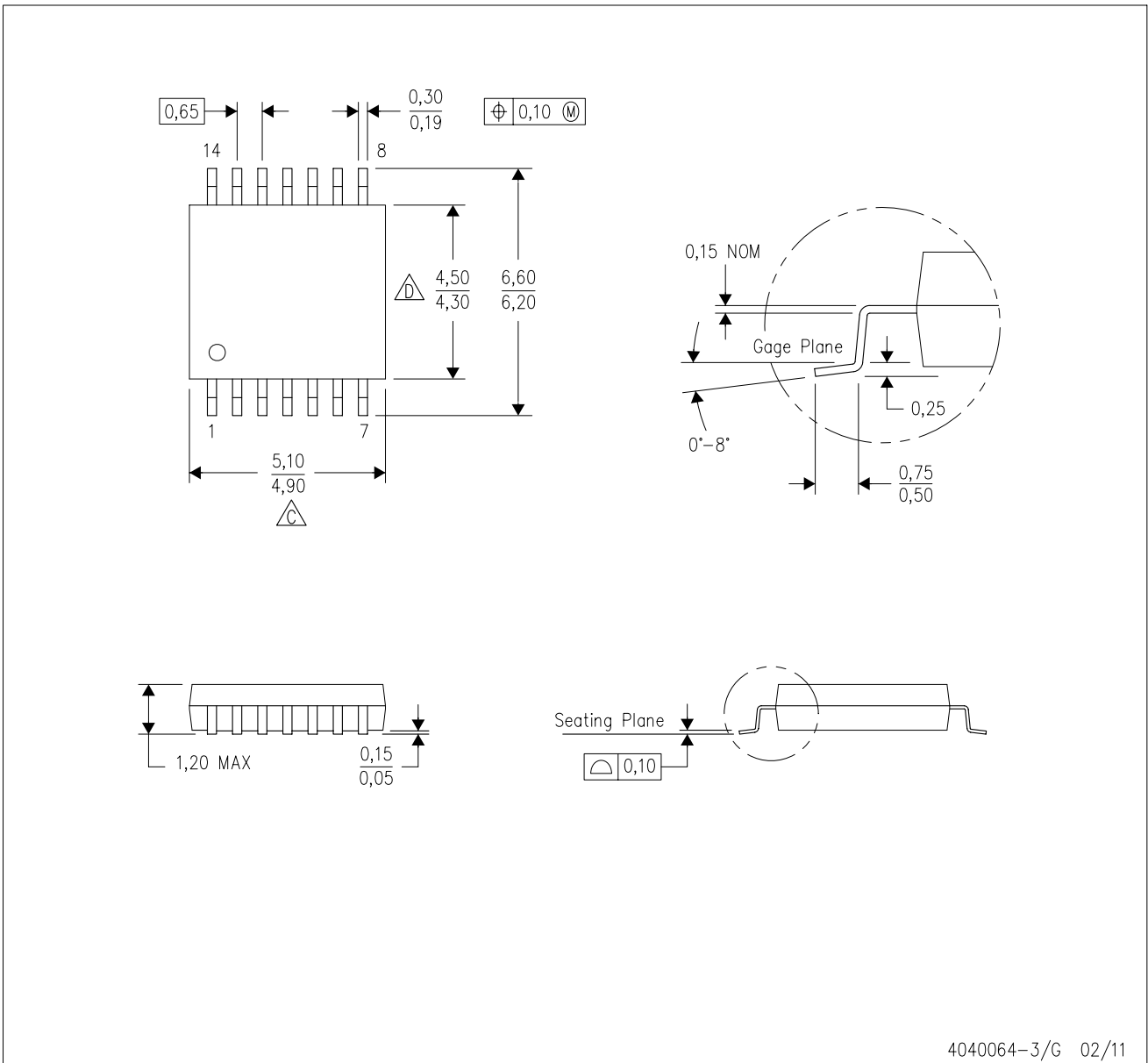
NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153



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PW (R−PDSO−G14)                                                PLASTIC  SMALL  OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

⊢⊣—12x0,65

⊢⊣— 14x0,30

14x1,55

⊢⊣—12x0,65

5,60

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

⊢——0,35

1,60

Example
Solder Mask Opening
(See Note E)

⊢—0,07
All Around

4211284−2/G  08/15

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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## N (R−PDIP−T**)

**PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN



| | PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|---|
| DIM | | | | | |
| A MAX | | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS−001 VARIATION | | AA | BB | AC | AD |

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14) ⚠D

0.045 (1,14) / 0.030 (0,76) ⚠D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option ⚠D

4040049/E  12/2002

NOTES:  A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.
⚠C  Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
⚠D  The 20 pin end lead shoulder width is a vendor option, either half or full width.