Atmel

ATtiny45

Appendix A - ATtiny45 Automotive specification at 150°C

DATASHEET

Description

This document contains information specific to devices operating at temperatures up to 150°C. Only deviations are covered in this appendix, all other information can be found in the complete Automotive datasheet. The complete Automotive datasheet can be found on www.atmel.com

1. Electrical Characteristics

1.1 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Min.	Typ.	Max.	Unit
Operating temperature	–55		+150	°C
Storage temperature	–65		+175	°C
Voltage on any pin except $\overline{RESET}$ with respect to ground	–0.5		V_{CC} + 0.5	V
Voltage on $\overline{RESET}$ with respect to ground	–0.5		+13.0	V
Maximum operating voltage			6.0	V
DC current per I/O pin		30.0		mA
DC current V_{CC} and GND pins		200.0		mA

1.2 DC Characteristics

T_A = –40°C to +150°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)(6)

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input low voltage, except XTAL1 and $\overline{RESET}$ pin	V_{CC} = 2.7V - 5.5V	V_{IL}	–0.5		$0.3V_{CC}$(1)	V
Input high voltage, except XTAL1 and $\overline{RESET}$ pins	V_{CC} = 2.7V - 5.5V	V_{IH}	$0.6V_{CC}$(2)		V_{CC} + 0.5	V
Input low voltage, XTAL1 pin	V_{CC} = 2.7V - 5.5V	V_{IL1}	–0.5		$0.1V_{CC}$(1)	V
Input high voltage, XTAL1 pin	V_{CC} = 2.7V - 5.5V	V_{IH1}	$0.7V_{CC}$(2)		V_{CC} + 0.5	V
Input low voltage, $\overline{RESET}$ pin	V_{CC} = 2.7V - 5.5V	V_{IL2}	–0.5		$0.2V_{CC}$(1)	V
Input high voltage, $\overline{RESET}$ pin	V_{CC} = 2.7V - 5.5V	V_{IH2}	$0.9V_{CC}$(2)		V_{CC} + 0.5	V
Input low voltage, $\overline{RESET}$ pin as I/O	V_{CC} = 2.7V - 5.5V	V_{IL3}	–0.5		$0.3V_{CC}$(1)	V
Input high voltage, $\overline{RESET}$ pin as I/O	V_{CC} = 2.7V - 5.5V	V_{IH3}	$0.6V_{CC}$(2)		V_{CC} + 0.5	V
Output low voltage(3), I/O pin except RESET	I_{OL} = 10mA, V_{CC} = 5V I_{OL} = 5mA, V_{CC} = 3V	V_{OL}			0.8 0.5	V
Output high voltage(4), I/O pin except RESET	I_{OH} = –10mA, V_{CC} = 5V I_{OH} = –5mA, V_{CC} = 3V	V_{OH}	4.0 2.2			V
Input leakage current I/O pin	V_{CC} = 5.5V, pin low (absolute value)	I_{IL}			1	µA
Input leakage current I/O pin	V_{CC} = 5.5V, pin high (absolute value)	I_{IH}			1	µA
Reset pull-up resistor		R_{RST}	30		60	kΩ
I/O pin pull-up resistor		R_{PU}	20		50	kΩ

1.2 DC Characteristics (Continued)

T_A = –40°C to +150°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)[6]

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Power supply current[6]	Active 4MHz, V_{CC} = 3V Active 8MHz, V_{CC} = 5V Active 16MHz, V_{CC} = 5V	I_{CC}			8 16 25	mA
	Idle 4MHz, V_{CC} = 3V Idle 8MHz, V_{CC} = 5V Idle 16MHz, V_{CC} = 5V	$I_{CC\ IDLE}$			6 12 14	mA
Power-down mode	WDT enabled, V_{CC} = 3V WDT enabled, V_{CC} = 5V	$I_{CC\ PWD}$[5]			90 140	µA
	WDT disabled, V_{CC} = 3V WDT disabled, V_{CC} = 5V				80 120	µA
Analog comparator input offset votage	V_{CC} = 5V V_{in} = $V_{CC}/2$	V_{ACIO}		<10	40	mV
Analog comparator input leakage current	V_{CC} = 5V V_{in} = $V_{CC}/2$	I_{ACLK}	–50		50	nA
Analog comparator propagation delay	V_{CC} = 4.0V	t_{ACPD}		500		ns

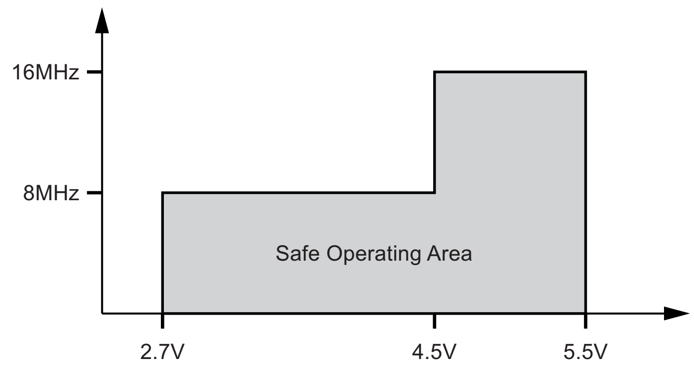
2. Memory Endurance

EEPROM endurance: 50,000 Write/Erase cycles

2.1 Maximum Speed versus V_{CC}

Maximum frequency is dependent on V_{CC}. As shown in Figure 2-1, the maximum frequency versus V_{CC} curve is linear between 2.7V < V_{CC} 4.5V[(6)].

Figure 2-1. Maximum Frequency versus V_{CC}



3. ADC Characteristics(6)

T_A = 125°C to 150°C, V_{CC} = 4.5V to 5.5V (unless otherwise noted)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Resolution				10		Bits
Absolute accuracy (Including INL, DNL, quantization error, gain and offset error)	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			2	3.5	LSB
	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz Noise reduction mode			2	3.5	LSB
Integral non-linearity (INL)	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz			0.6	2.5	LSB
Differential non-linearity (DNL)	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			0.30	1.0	LSB
Gain error	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz		–3.5	–1.3	3.5	LSB
Offset error	V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200kHz			1.8	3.5	LSB
Conversion time	Free running conversion		13 cycles			µs
Clock frequency			50		200	kHz
Analog supply voltage		AV_{CC}	V_{CC} – 0.3		V_{CC} + 0.3	V
Reference voltage		V_{REF}	1.0		AV_{CC}	V
Input voltage		V_{IN}	GND		V_{REF} – 50mV	V
Input bandwidth				38.5		kHz
Internal voltage reference		V_{INT}	1.0	1.1	1.2	V
Reference input resistance		R_{REF}	25.6	32	38.4	kΩ
Analog input resistance		R_{AIN}		100		MΩ

Notes:
1. "Max" means the highest value where the pin is guaranteed to be read as low
2. "Min" means the lowest value where the pin is guaranteed to be read as high
3. Although each I/O port can sink more than the test conditions (20mA at V_{CC} = 5V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all IOL, for all ports, should not exceed 400mA.
   2] The sum of all IOL, for ports C0 - C5, should not exceed 200mA.
   3] The sum of all IOL, for ports C6, D0 - D4, should not exceed 300mA.
   4] The sum of all IOL, for ports B0 - B7, D5 - D7, should not exceed 300mA.
   If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
4. Although each I/O port can source more than the test conditions (20mA at Vcc = 5V) under steady state conditions (non-transient), the following must be observed:
   1] The sum of all IOH, for all ports, should not exceed 400mA.
   2] The sum of all IOH, for ports C0 - C5, should not exceed 200mA.
   3] The sum of all IOH, for ports C6, D0 - D4, should not exceed 300mA.
   4] The sum of all IOH, for ports B0 - B7, D5 - D7, should not exceed 300mA.
   If IOH exceeds the test condition, VOH may exceed the related specification. Pins are not guaranteed to source current greater than the listed test condition.
5. Minimum V_{CC} for Power-down is 2.5V.

4. ATtiny45 Typical Characteristics

4.1 Active Supply Current

Figure 4-1. Active Supply Current versus Frequency (1 - 20 MHz)

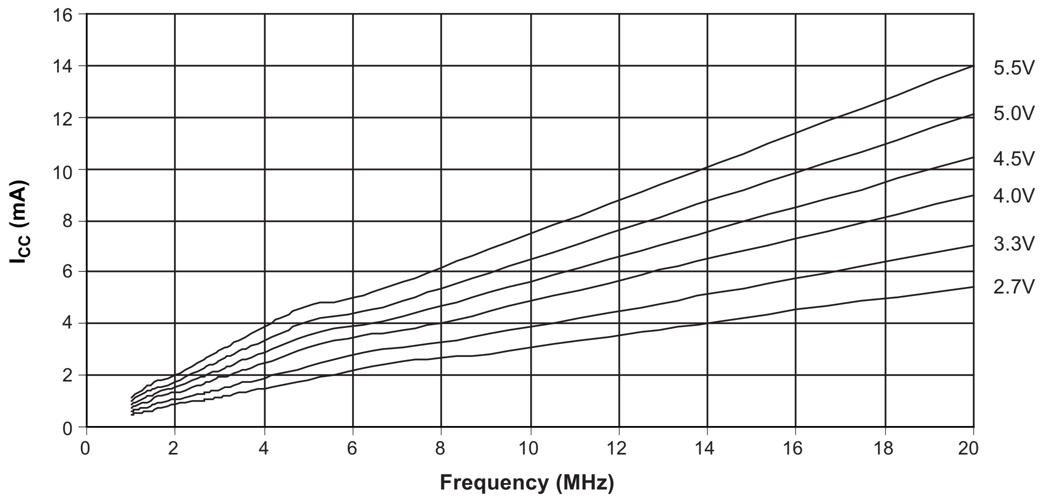
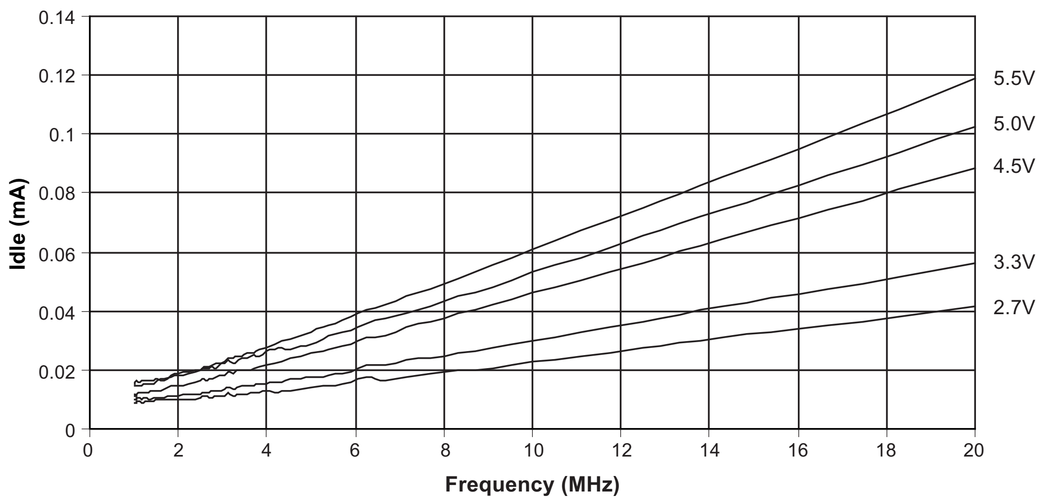


Figure 4-2. Idle Supply Current versus Frequency (1 - 20 MHz)



4.2 Power-Down Supply Current

Figure 4-3. Power-down Supply Current versus V_{CC} (Watchdog Timer Disabled)

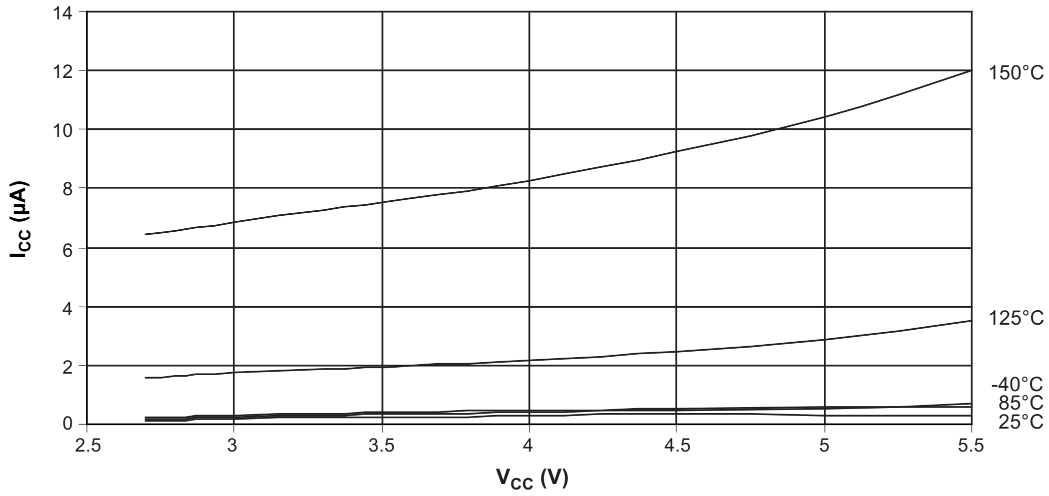
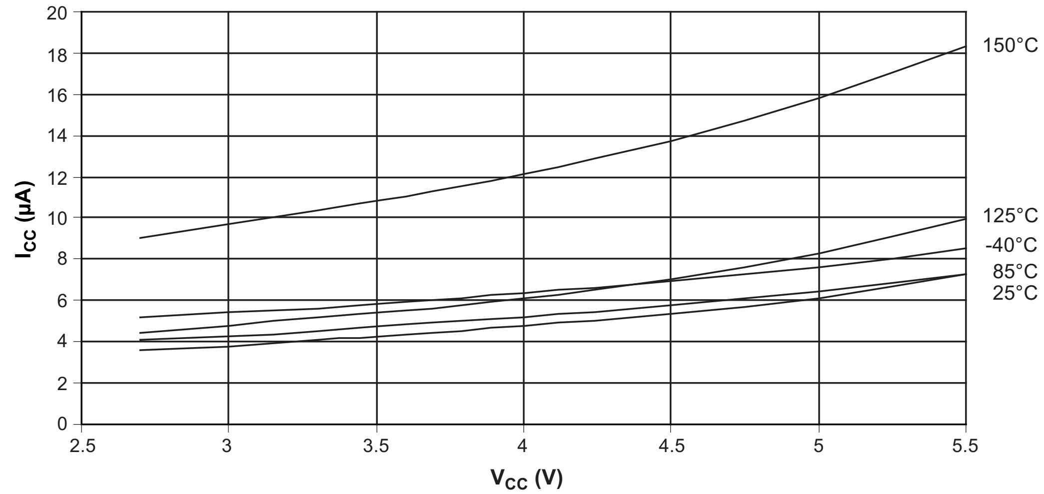


Figure 4-4. Power-down Supply Current versus V_{CC} (Watchdog Timer Enabled)



4.3 Pin Pull-up

Figure 4-5. I/O Pin Pull-up Resistor Current versus Input Voltage (V_{CC} = 5V)

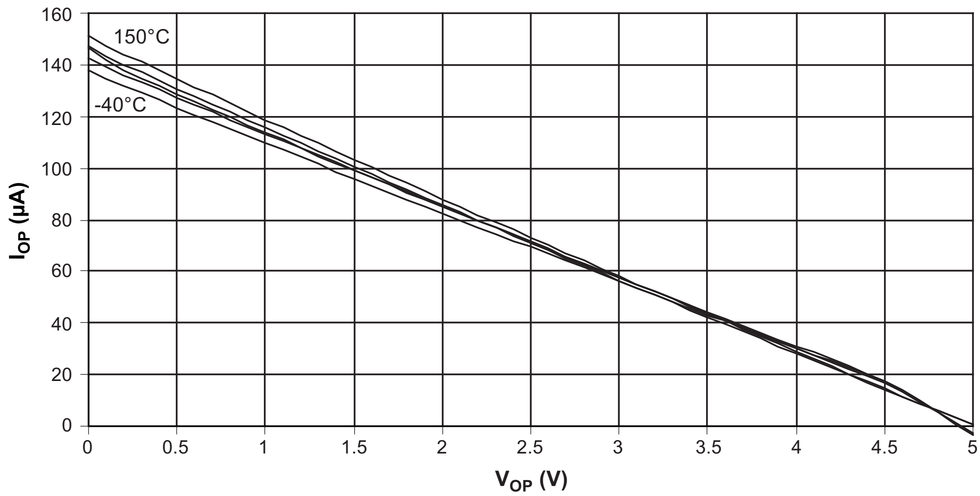


Figure 4-6. Output Low Voltage versus Output Low Current (V_{CC} = 5V)

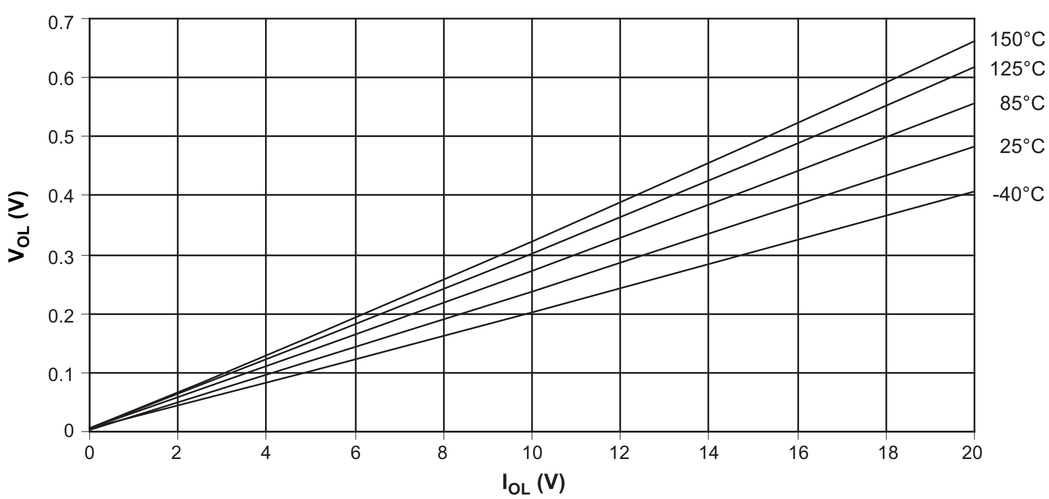


Figure 4-7. Output Low Voltage versus Output Low Current (V_{CC} = 3V)

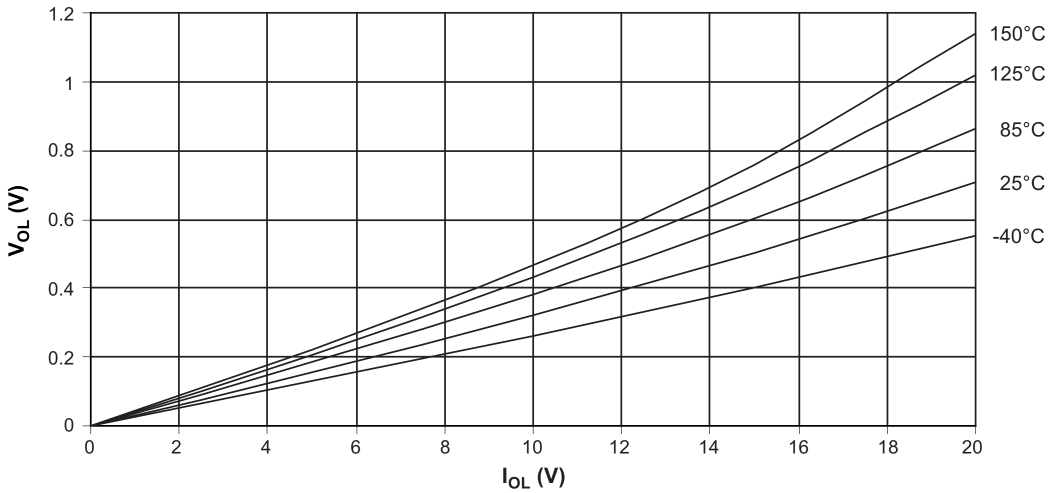


Figure 4-8. Output High Voltage versus Output High Current (V_{CC} = 5V)

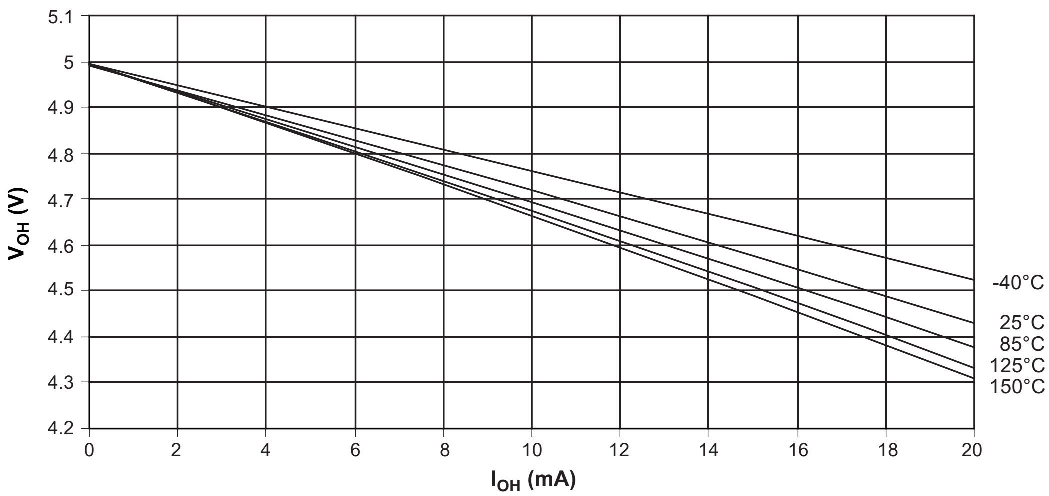


Figure 4-9. Output High Voltage versus Output High Current (V_{CC} = 3V)

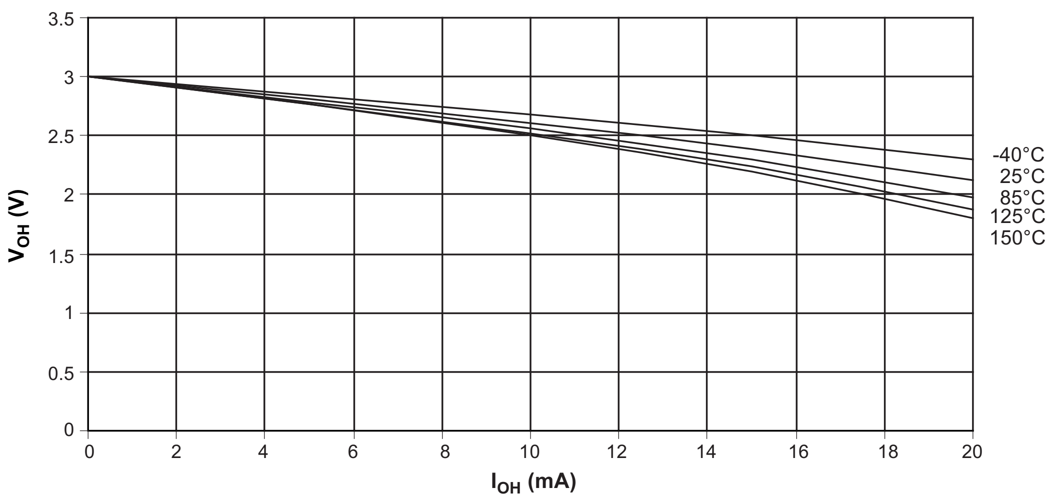
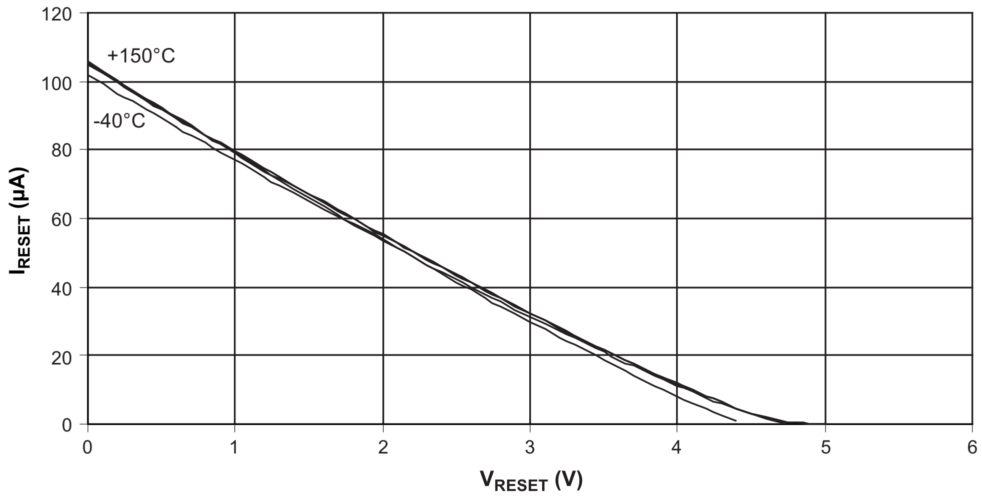


Figure 4-10. Reset Pull-Up Resistor Current versus Reset Pin Voltage (V_{CC} = 5V)



4.4 Pin Thresholds and Hysteresis

Figure 4-11. I/O Pin Input Threshold versus V_{CC} (VIH, I/O Pin Read as '1')

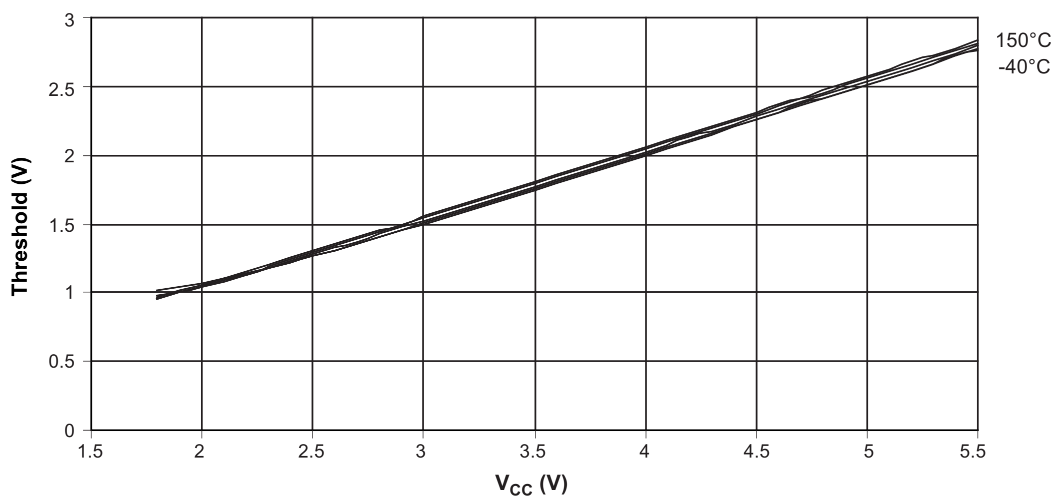


Figure 4-12. I/O Pin Input Threshold versus V_{CC} (VIL, I/O Pin Read as '0')

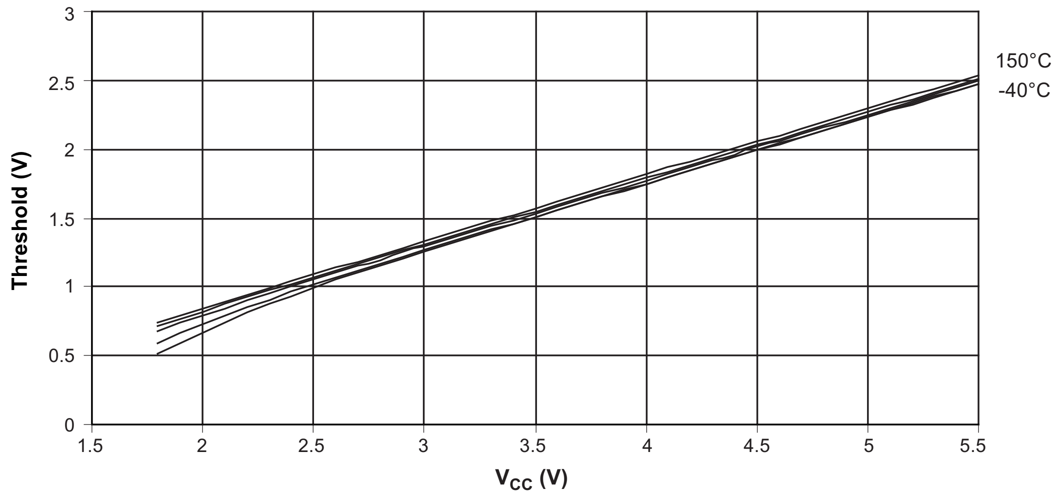


Figure 4-13. Reset Input Threshold Voltage versus V_{CC} (VIH, Reset Pin Read as '1')

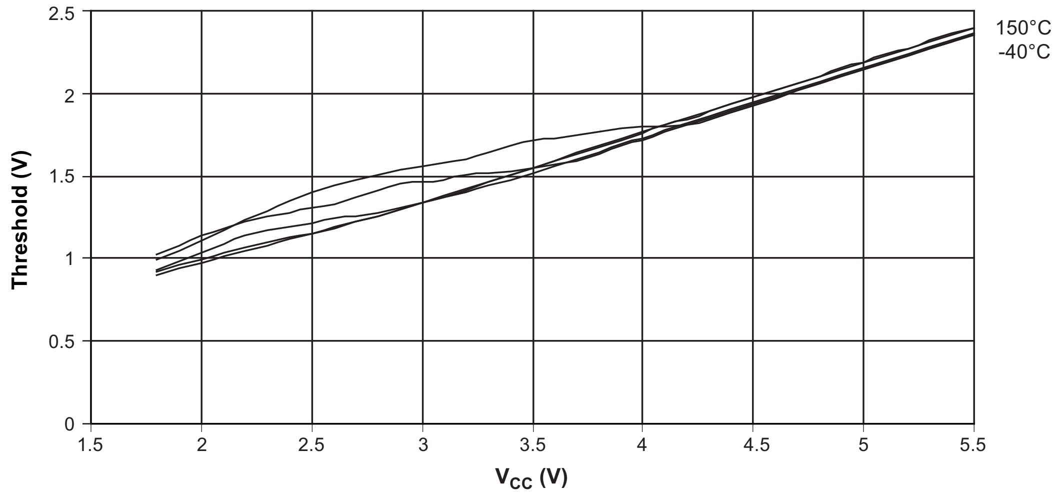
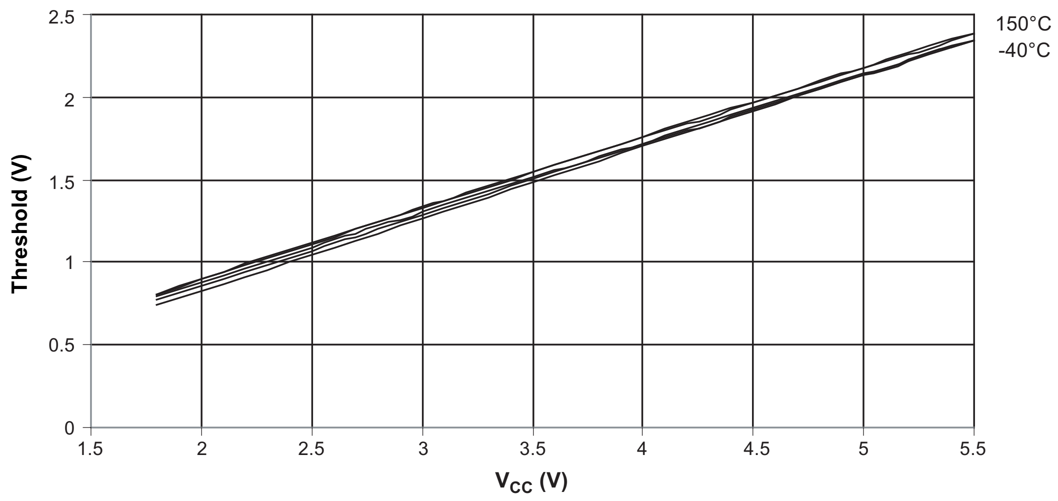


Figure 4-14. Reset Input Threshold Voltage versus V_{CC} (VIL, Reset Pin Read as '0')



4.5 Internal Oscillator Speed

Figure 4-15. Watchdog Oscillator Frequency versus V_{CC}

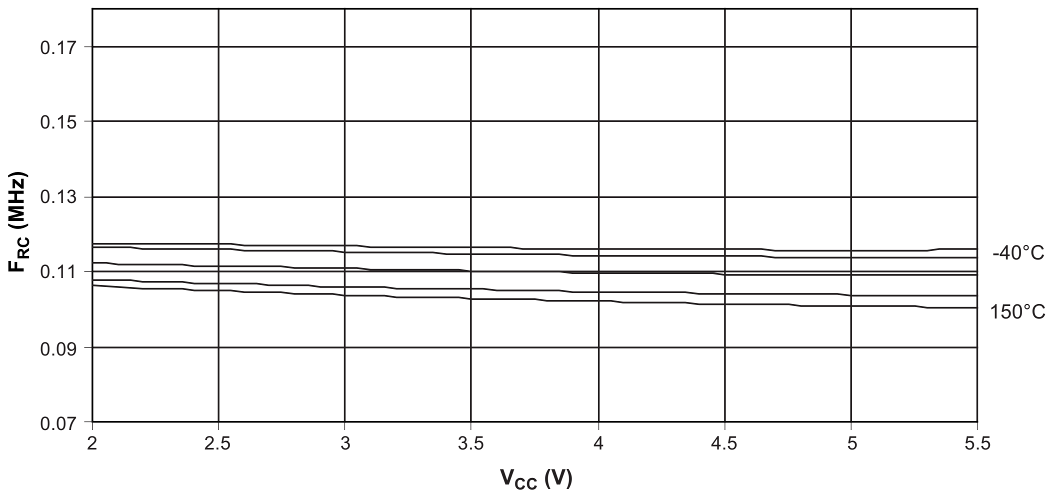


Figure 4-16. Calibrated 8 MHz RC Oscillator Frequency versus Temperature

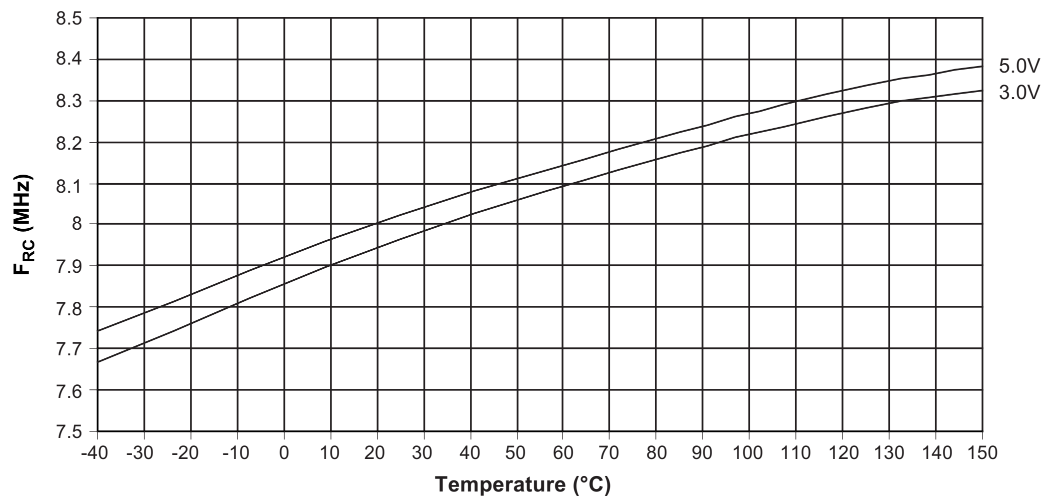


Figure 4-17. Calibrated 8 MHz RC Oscillator Frequency versus V_{CC}

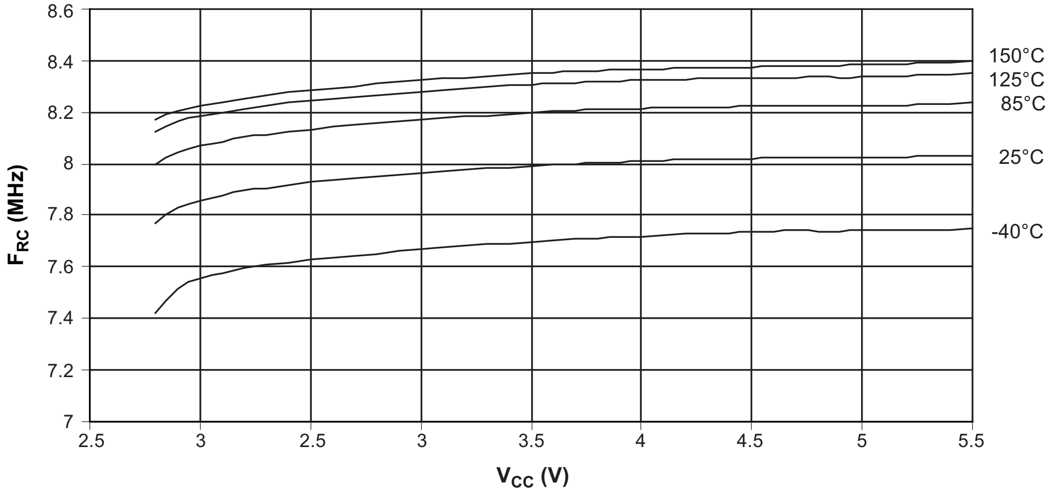
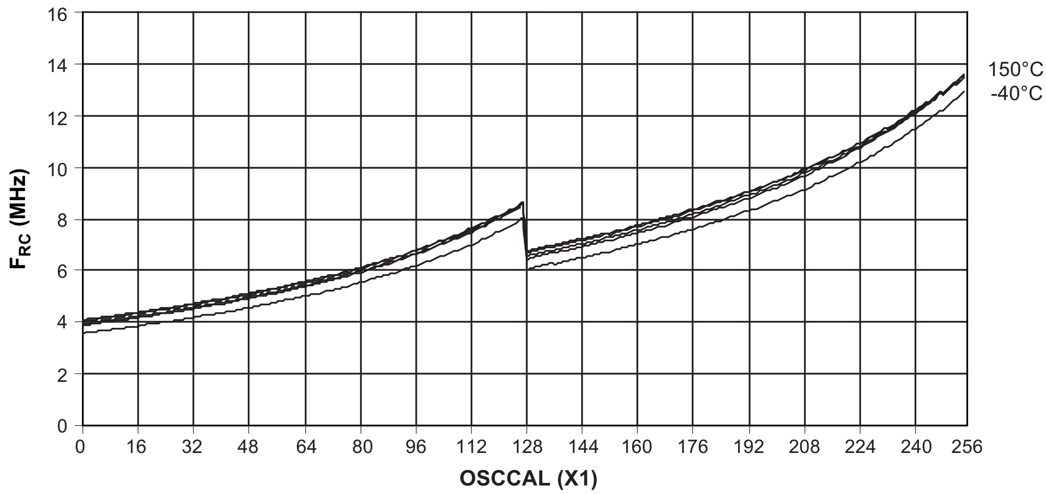


Figure 4-18. Calibrated 8 MHz RC Oscillator Frequency versus OSCCAL Value



4.6 BOD Thresholds and Analog Comparator Offset

Figure 4-19. BOD Threshold versus Temperature (BODLEVEL is 4.3V)

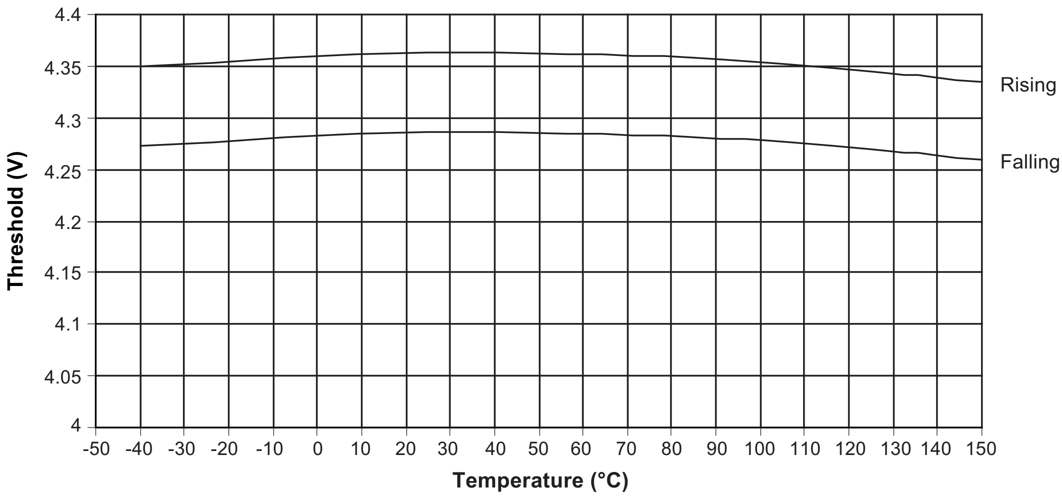


Figure 4-20. BOD Threshold versus Temperature (BODLEVEL is 2.7V)

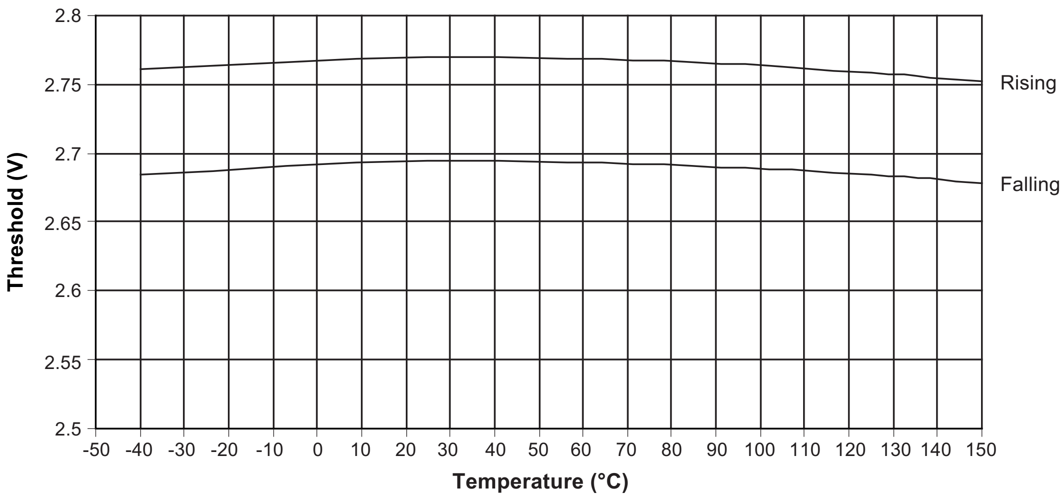
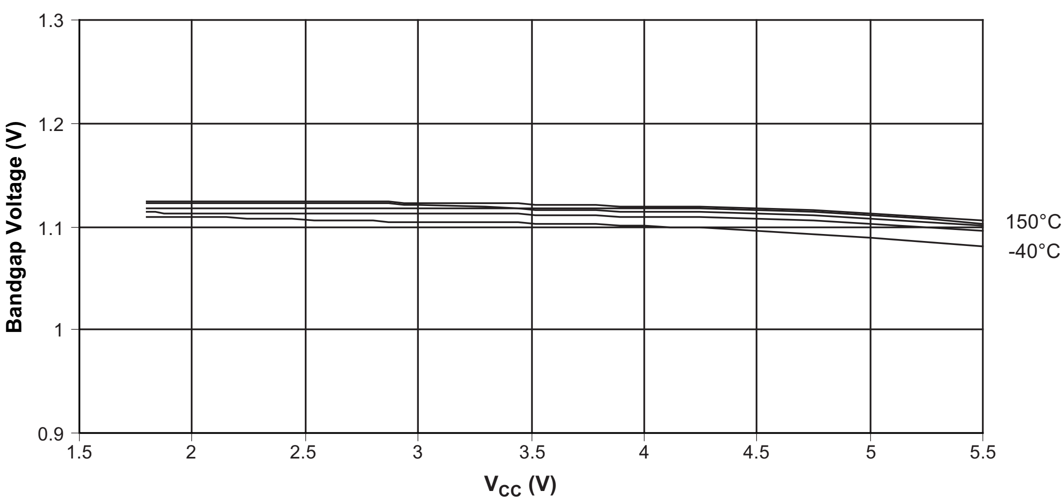


Figure 4-21. Bandgap Voltage versus V_{CC}



4.7 Peripheral Units

Figure 4-22. Analog to Digital Converter GAIN versus Temperature, Single Ended

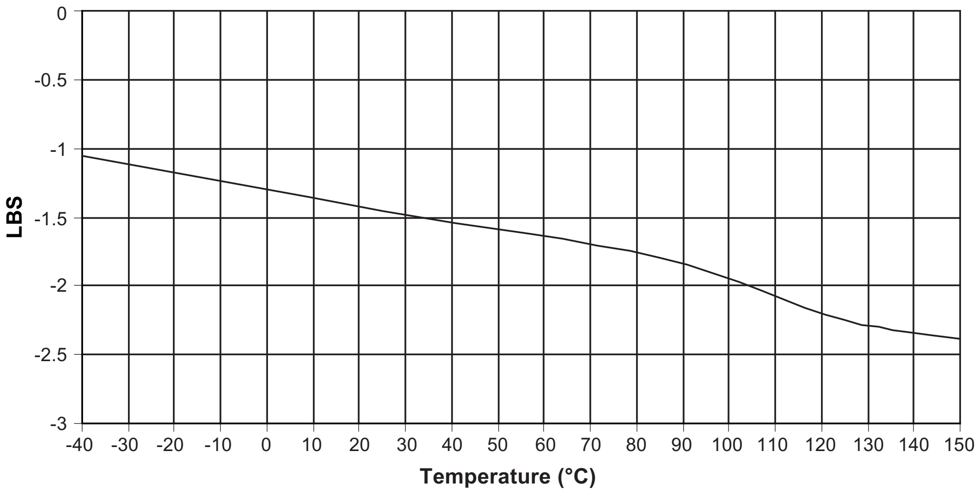


Figure 4-23. Analog to Digital Converter GAIN versus Temperature, Differential Mode

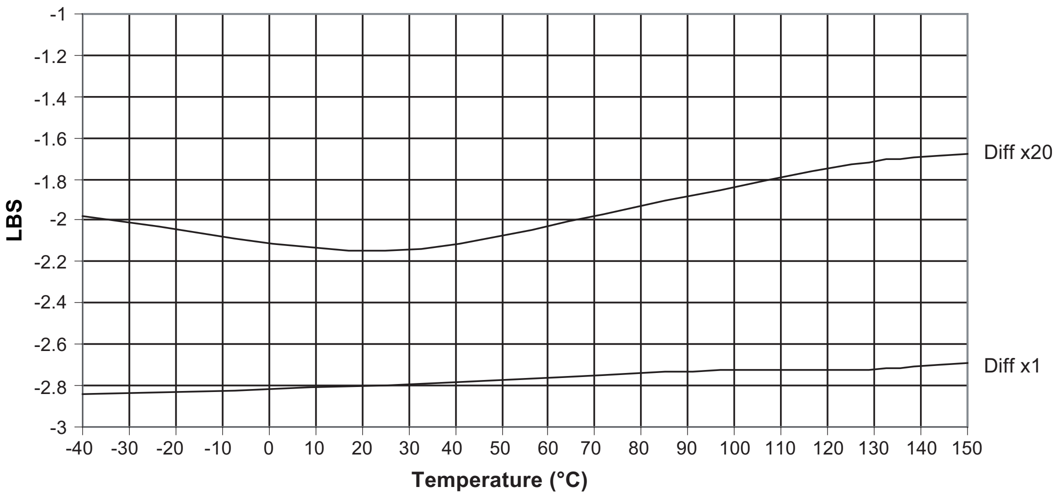


Figure 4-24. Analog to Digital Converter OFFSET versus Temperature, Single Ended

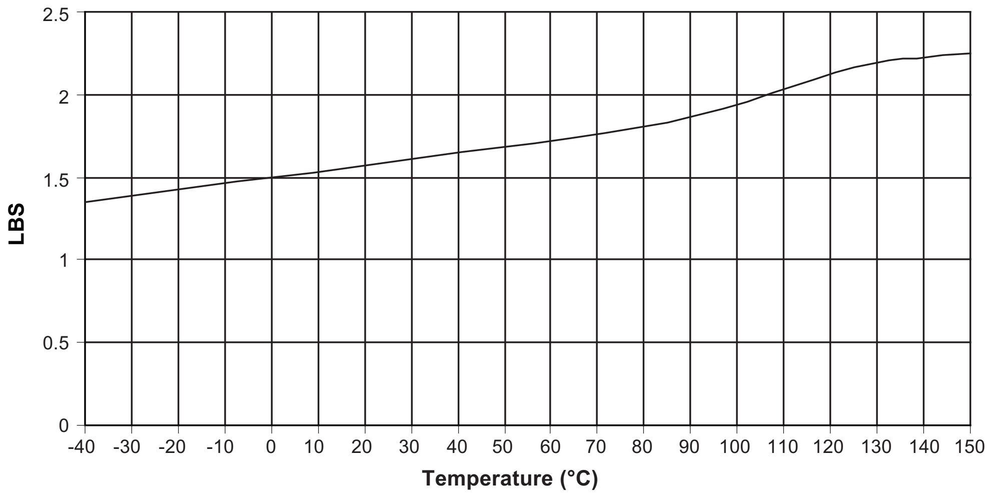


Figure 4-25. Analog to Digital Converter OFFSET versus Temperature, Differential Mode

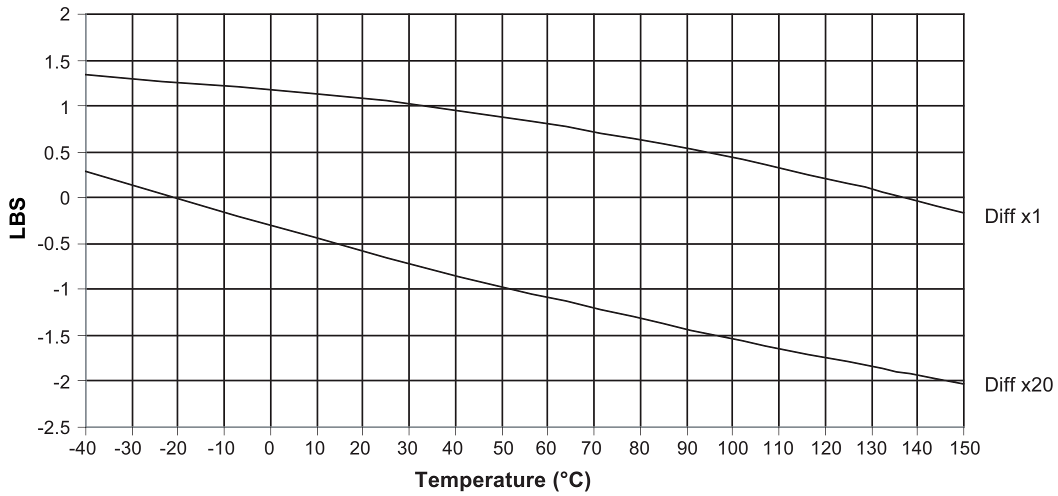


Figure 4-26. Analog to Digital Converter DNL versus Temperature, Single Ended

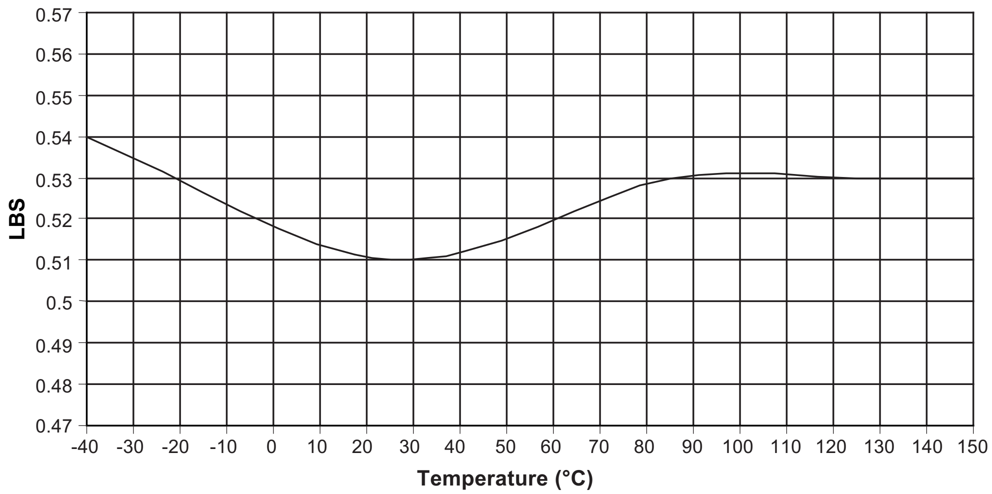


Figure 4-27. Analog to Digital Converter DNL versus Temperature, Differential Mode

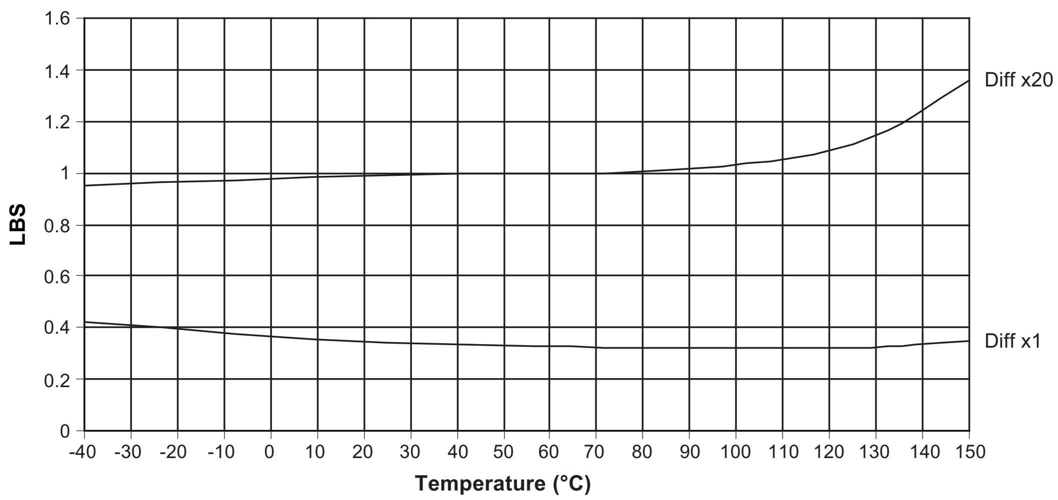


Figure 4-28. Analog to Digital Converter INL versus Temperature, Single Ended

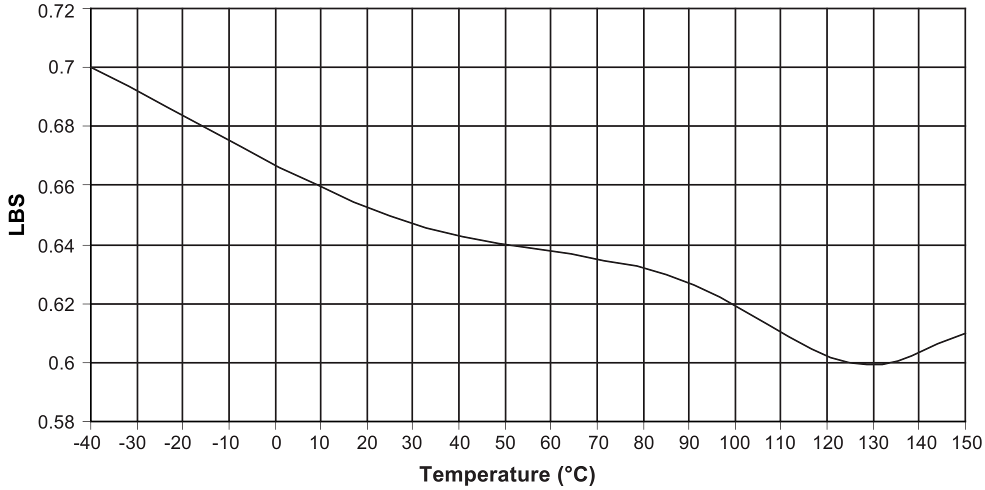
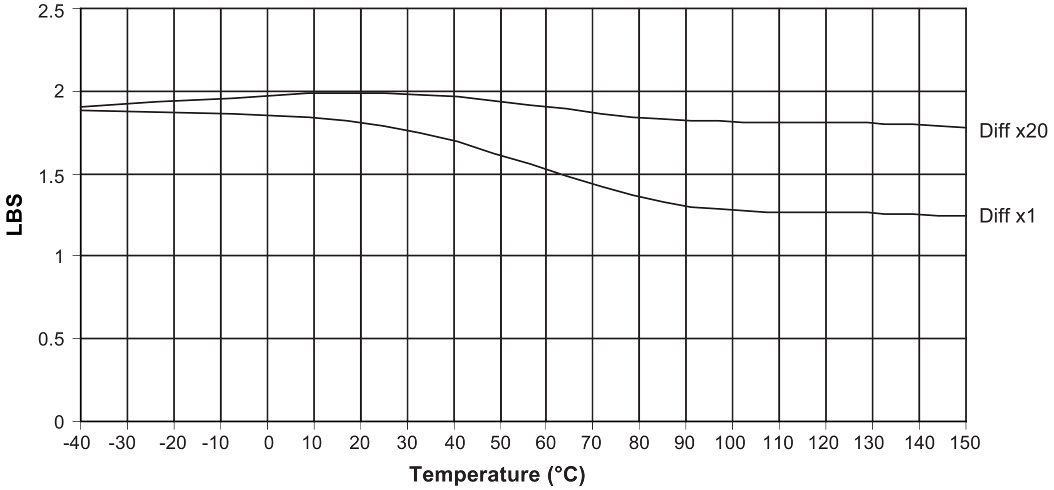


Figure 4-29. Analog to Digital Converter INL versus Temperature, Differential Mode



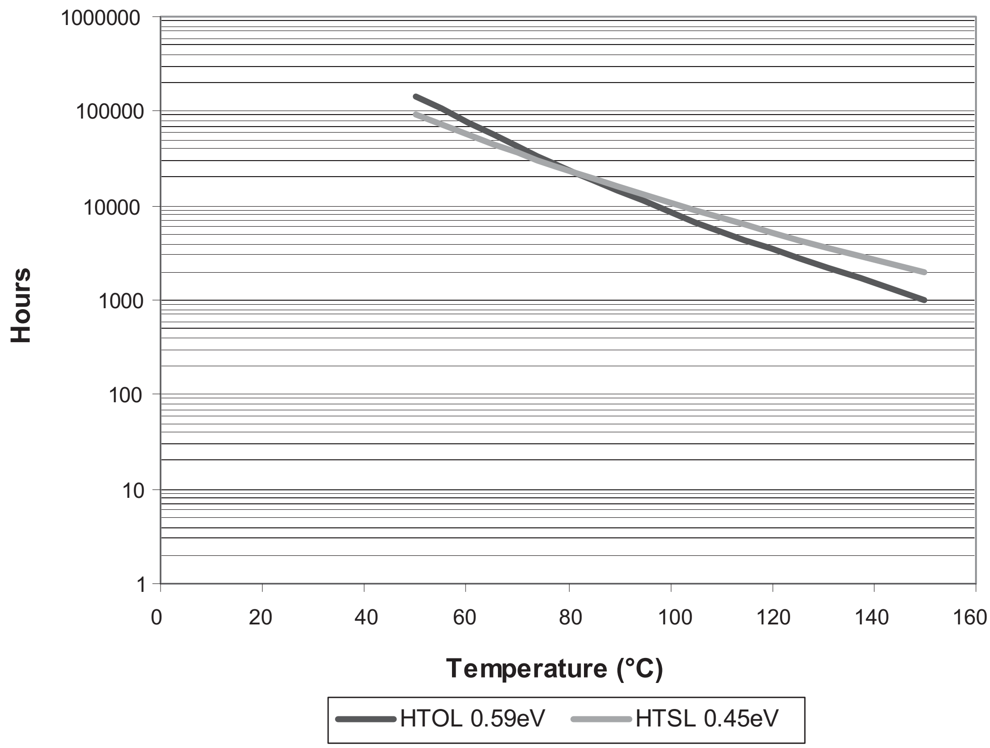
5. Grade 0 Qualification

The ATtiny45 has been developed and manufactured according to the most stringent quality assurance requirements of ISO-TS-16949 and verified during product qualification as per AEC-Q100 grade 0.

AEC-Q100 qualification relies on temperature accelerated stress testing. High temperature field usage however may result in less significant stress test acceleration. In order to prevent the risk that ATtiny45 lifetime would not satisfy the application end-of-life reliability requirements, Atmel has extended the testing, whenever applicable (high temperature operating life test, high temperature storage life, data retention, thermal cycles), far beyond the AEC-Q100 requirements. Thereby, Atmel® verified the ATtiny45 has a long safe lifetime period after the grade 0 qualification acceptance limits.

The valid domain calculation depends on the activation energy of the potential failure mechanism that is considered. Examples are given in figure 1. Therefore any temperature mission profile which could exceed the AEC-Q100 equivalence domain shall be submitted to Atmel for a thorough reliability analysis.

Figure 5-1. AEC-Q100 Lifetime Equivalence



6. Ordering Information

6.1 ATtiny45

Table 6-1. ATtiny45

Speed (MHz)	Power Supply	Ordering Code	Package[1]	Operation Range
16[2]	2.7 - 5.5V	ATtiny45-15MT2	PC	Extended (–40°C to +150°C)

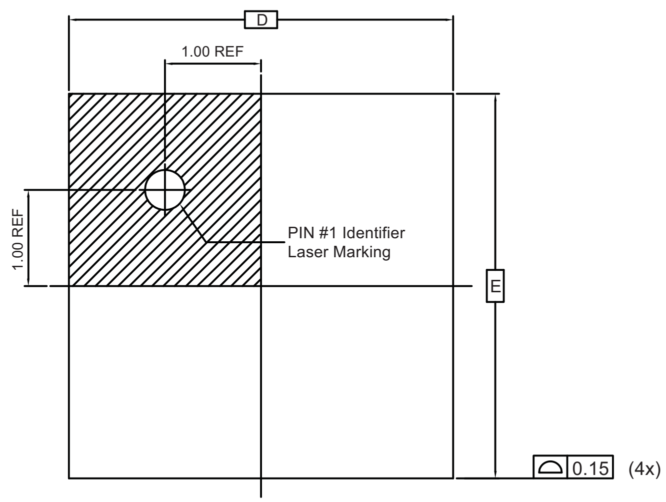
Notes: 1. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also halide free and fully green.

2. For speed versus V_{CC}, see Figure 2-1 on page 4 and complete product datasheet.

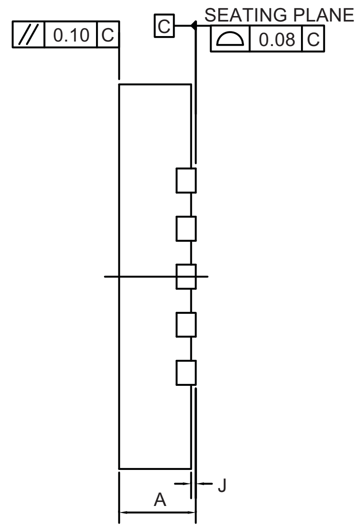
Table 6-2. Package Information

Package Type	
PC	20-lead, 4.0x 4.0mm body, lead pitch 0.60mm, quad flat no-lead package

Figure 6-1. Package PC

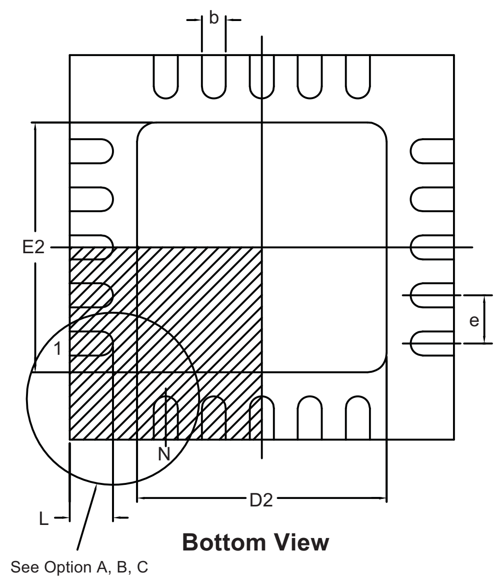


Top View



Side View

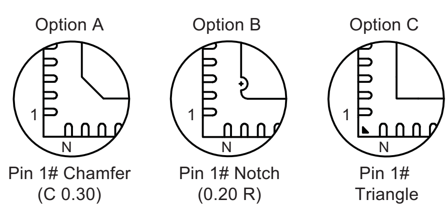
DRAWINGS NOT SCALED



Bottom View

COMMON DIMENSIONS IN MM

SYMBOL	MIN.	NOM.	MAX.	NOTES
A	0.70	0.75	0.80	
J	0.00	----	0.05	
D/E	3.90	4.00	4.10	
D2/E2	2.50	2.60	2.70	
N		20		
e		0.50 BSC		
L	0.35	0.45	0.55	
b	0,20	0.25	0.30	



Compliant JEDEC Standard MO-220 Variation WGGD-5

06/25/09

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** packagedrawings@atmel.com	PC, 20-Lead - 4.0x4.0mm Body, 0.50mm Pitch Quad Flat No Lead Package (QFN)		PC	I

7. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
7696D-AVR-06/14	• Put datasheet in the latest template
7696C-AVR-10/12	• Figure 6-1 “Package PC” on page 23 updated
7696B-AVR-04/09	• Added EEPROM endurance. See Section 2. “Memory Endurance” on page 4.

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